JAN 18 2005
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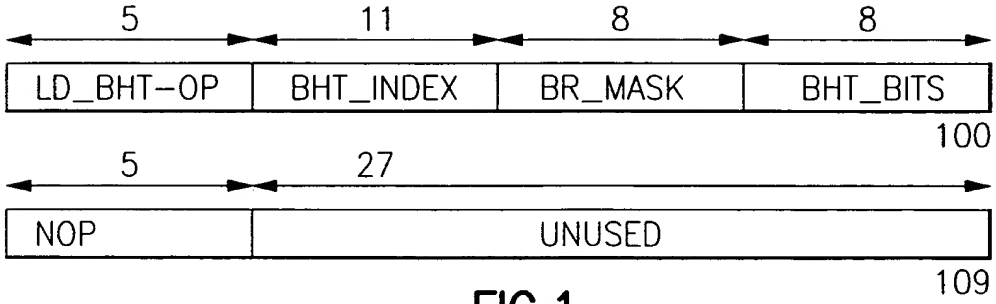


FIG.1

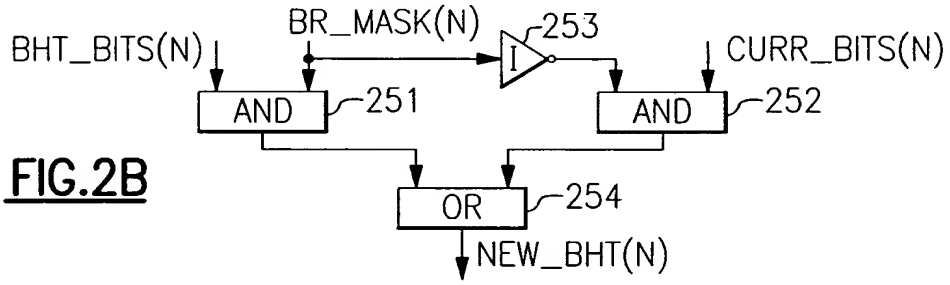
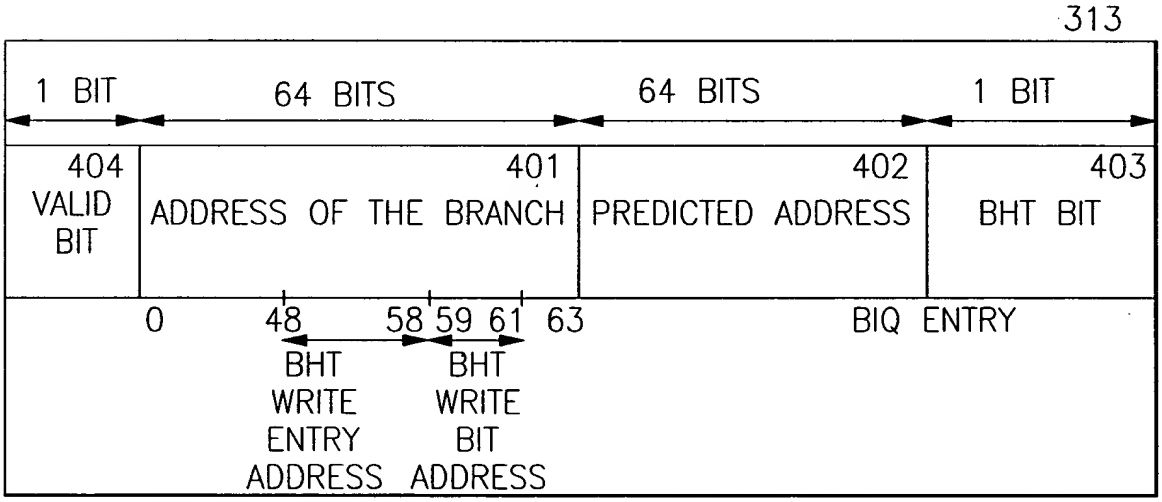
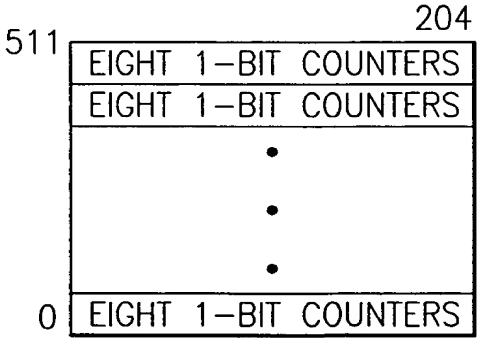


FIG.2B



BRANCH INFORMATION QUEUE (BIQ)

FIG.4



BHT

FIG.5

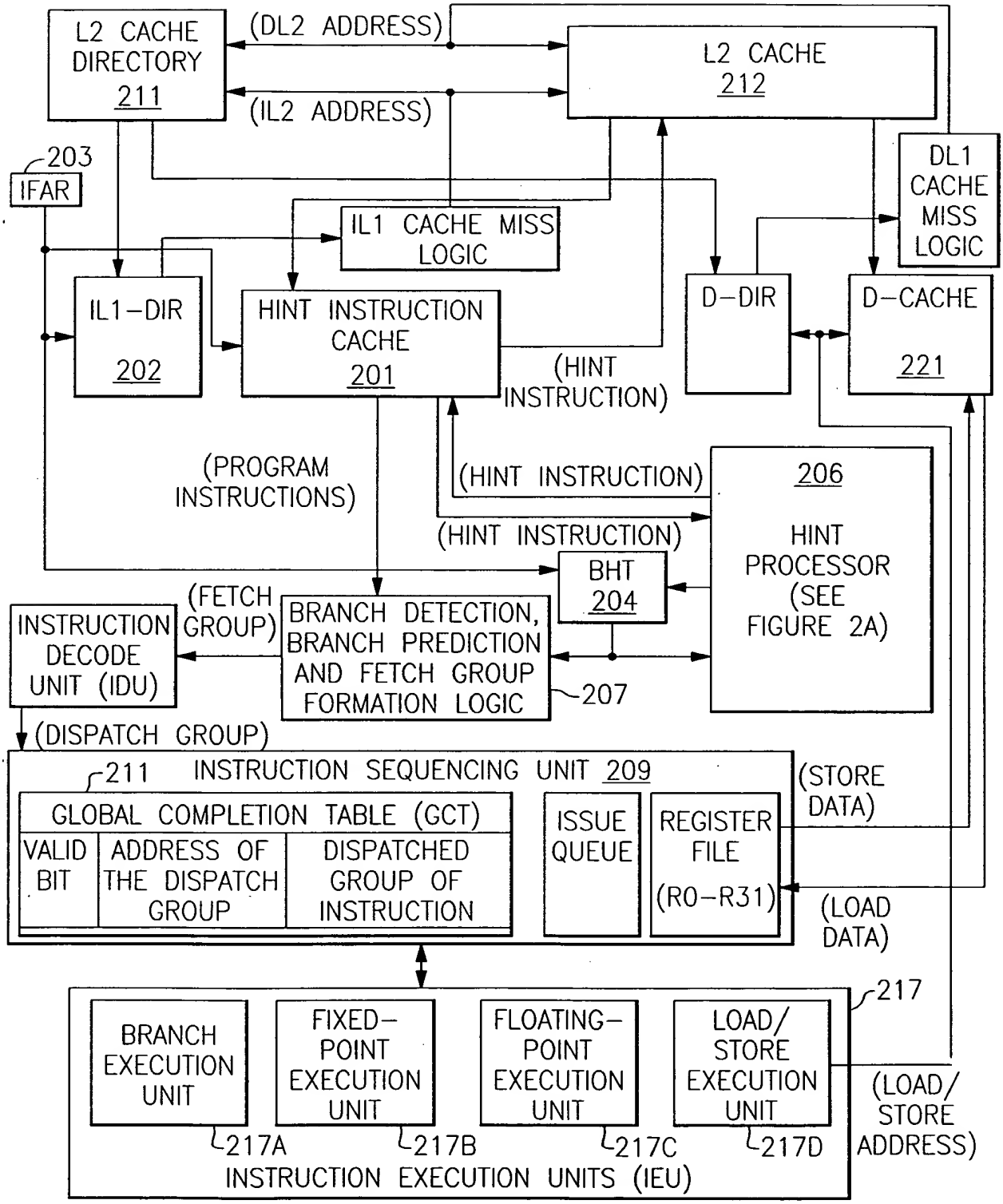

L2 CACHE DIRECTORY 211
(DL2 ADDRESS)
(IL2 ADDRESS)
L2 CACHE 212
203
IFAR
IL1 CACHE MISS LOGIC
DL1 CACHE MISS LOGIC
IL1-DIR 202
HINT INSTRUCTION CACHE 201
D-DIR
D-CACHE 221
(HINT INSTRUCTION)
(PROGRAM INSTRUCTIONS)
(HINT INSTRUCTION)
(HINT INSTRUCTION)
206
HINT PROCESSOR (SEE FIGURE 2A)
BHT 204
(FETCH GROUP)
INSTRUCTION DECODE UNIT (IDU)
BRANCH DETECTION, BRANCH PREDICTION AND FETCH GROUP FORMATION LOGIC
207
(DISPATCH GROUP)
211
INSTRUCTION SEQUENCING UNIT 209
(STORE DATA)
GLOBAL COMPLETION TABLE (GCT)
VALID BIT
ADDRESS OF THE DISPATCH GROUP
DISPATCHED GROUP OF INSTRUCTION
ISSUE QUEUE
REGISTER FILE (R0-R31)
(LOAD DATA)
217
BRANCH EXECUTION UNIT
FIXED-POINT EXECUTION UNIT
FLOATING-POINT EXECUTION UNIT
LOAD/STORE EXECUTION UNIT
(LOAD/STORE ADDRESS)
217A
217B
217C
217D
INSTRUCTION EXECUTION UNITS (IEU)

FIG.2

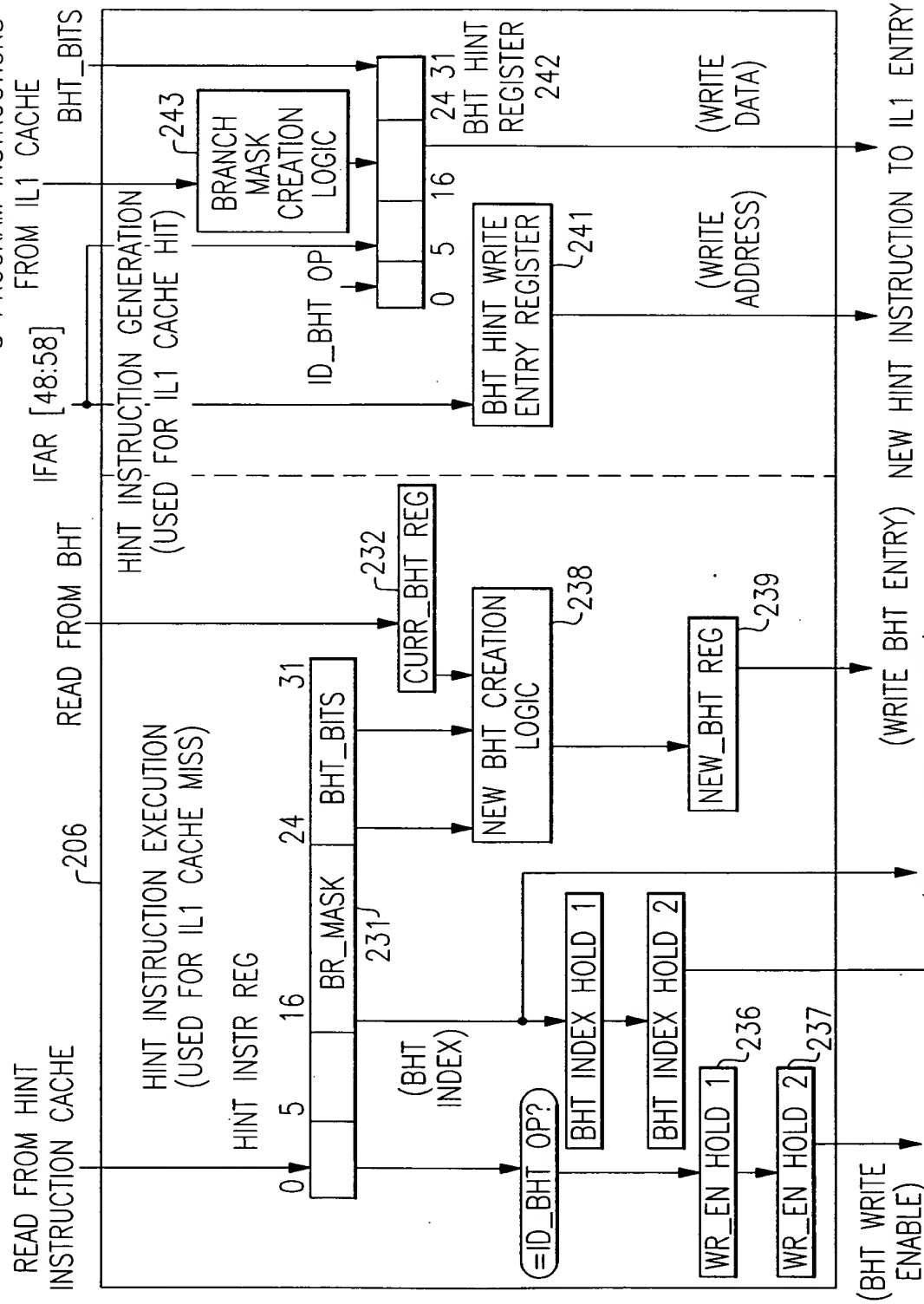

8 PROGRAM INSTRUCTIONS FROM IL1 CACHE
BHT_BITS
IFAR [48:58]
READ FROM BHT
HINT INSTRUCTION GENERATION (USED FOR IL1 CACHE HIT)
243
BRANCH MASK CREATION LOGIC
ID_BHT OP
24 31
BHT HINT REGISTER 242
0 5 16
BHT HINT WRITE ENTRY REGISTER
241
(WRITE DATA)
(WRITE ADDRESS)
232
CURR_BHT REG
238
NEW BHT CREATION LOGIC
239
NEW_BHT REG
(WRITE BHT ENTRY)
NEW HINT INSTRUCTION TO IL1 ENTRY
(BHT INDEX TO READ)
(BHT INDEX TO WRITE)
206
HINT INSTRUCTION EXECUTION (USED FOR IL1 CACHE MISS)
HINT INSTR REG
31
24
16
5
0
BHT_BITS
BR_MASK
231
(BHT INDEX)
READ FROM HINT INSTRUCTION CACHE
=ID_BHT OP?
BHT INDEX HOLD 1
BHT INDEX HOLD 2
WR_EN HOLD 1
236
WR_EN HOLD 2
237
(BHT WRITE ENABLE)

FIG.2A

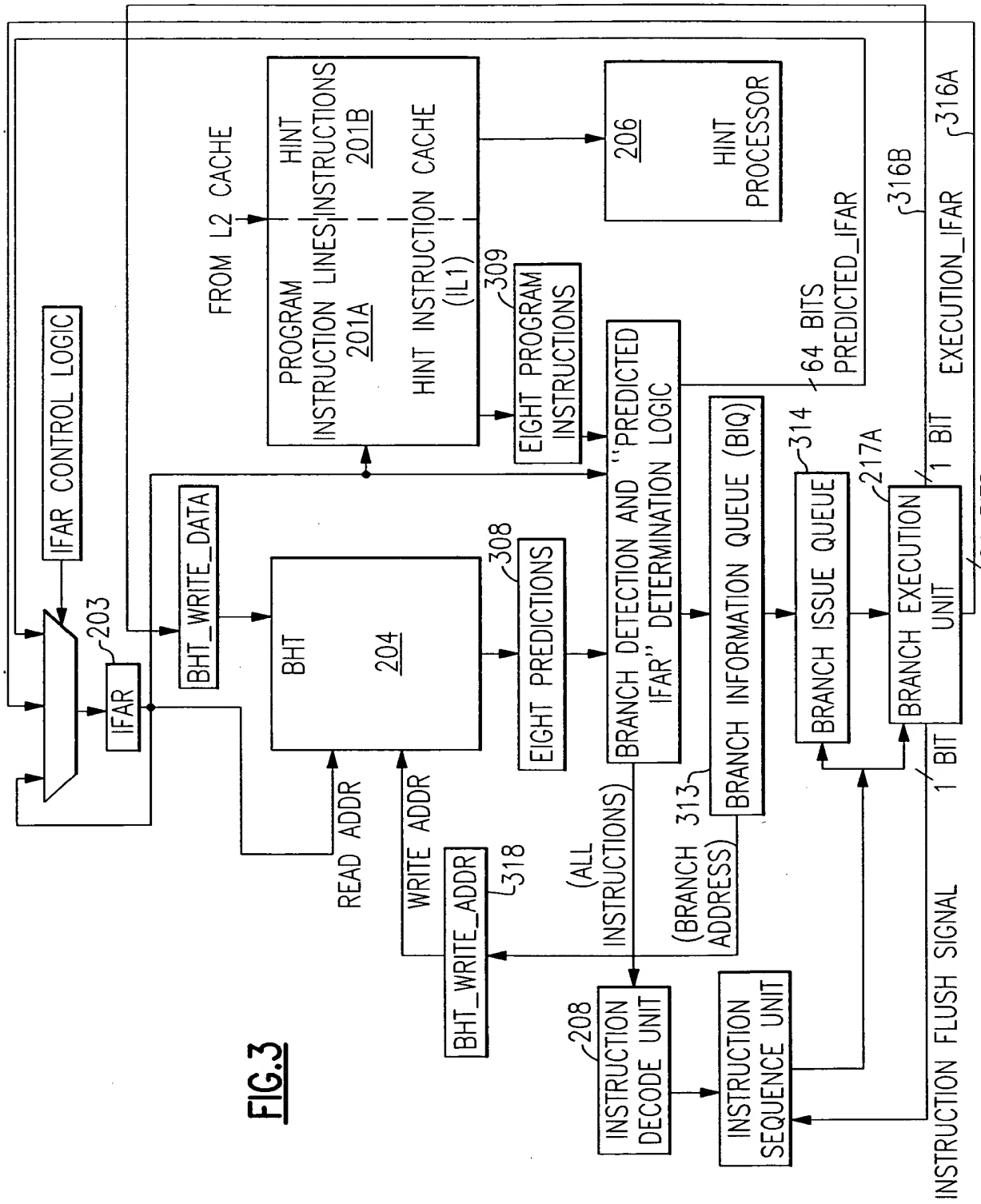

IFAR CONTROL LOGIC
203
IFAR
BHT_WRITE_DATA
BHT
204
READ ADDR
WRITE ADDR
BHT_WRITE_ADDR
318
308
EIGHT PREDICTIONS
FROM L2 CACHE
PROGRAM INSTRUCTION LINES
201A
HINT INSTRUCTIONS
201B
HINT INSTRUCTION CACHE
(IL1)
309
EIGHT PROGRAM INSTRUCTIONS
206
HINT PROCESSOR
BRANCH DETECTION AND "PREDICTED IFAR" DETERMINATION LOGIC
64 BITS PREDICTED_IFAR
316B
316A
1 BIT EXECUTION_IFAR
BRANCH INFORMATION QUEUE (BIQ)
314
BRANCH ISSUE QUEUE
217A
BRANCH EXECUTION UNIT
64 BITS
(ALL INSTRUCTIONS)
(BRANCH ADDRESS)
313
208
INSTRUCTION DECODE UNIT
INSTRUCTION SEQUENCE UNIT
1 BIT
INSTRUCTION FLUSH SIGNAL

FIG.3

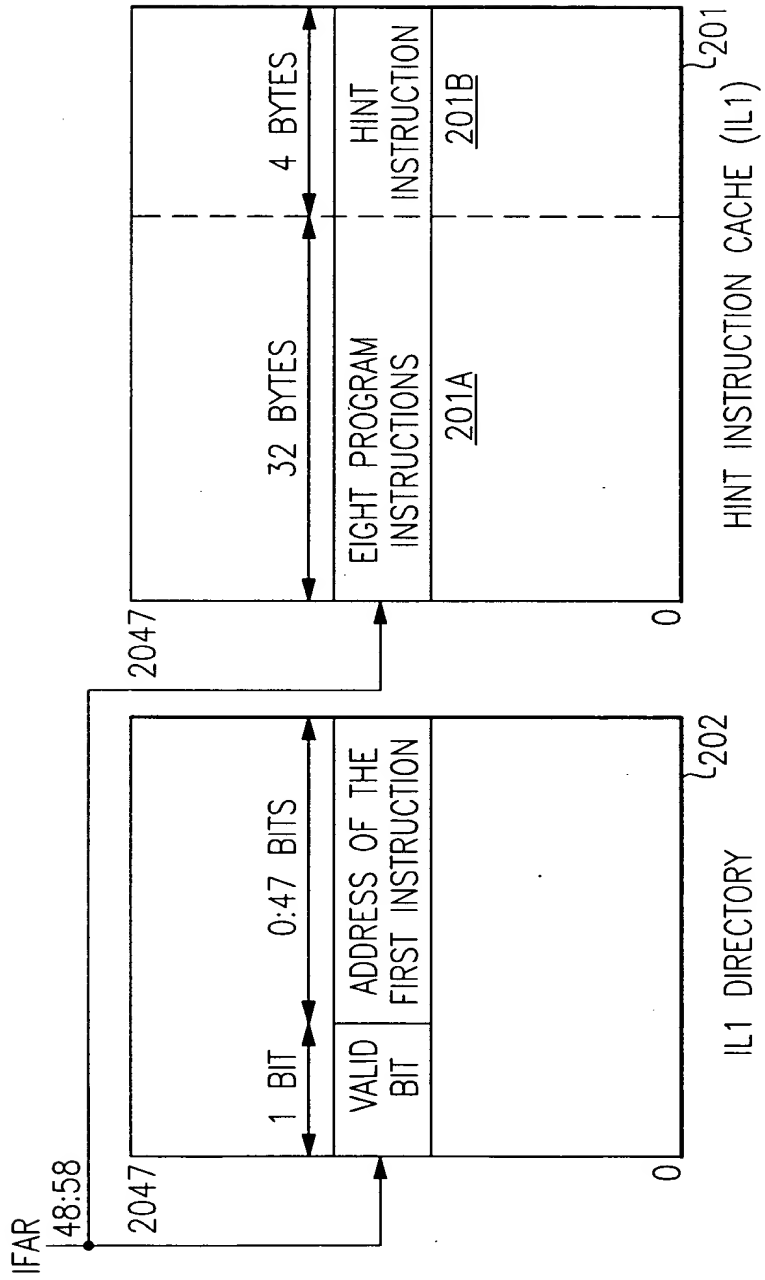

IFAR
48:58
2047
0
1 BIT
0:47 BITS
VALID BIT
ADDRESS OF THE FIRST INSTRUCTION
IL1 DIRECTORY
202
2047
0
32 BYTES
4 BYTES
EIGHT PROGRAM INSTRUCTIONS
HINT INSTRUCTION
201A
201B
HINT INSTRUCTION CACHE (IL1)
201

FIG.6

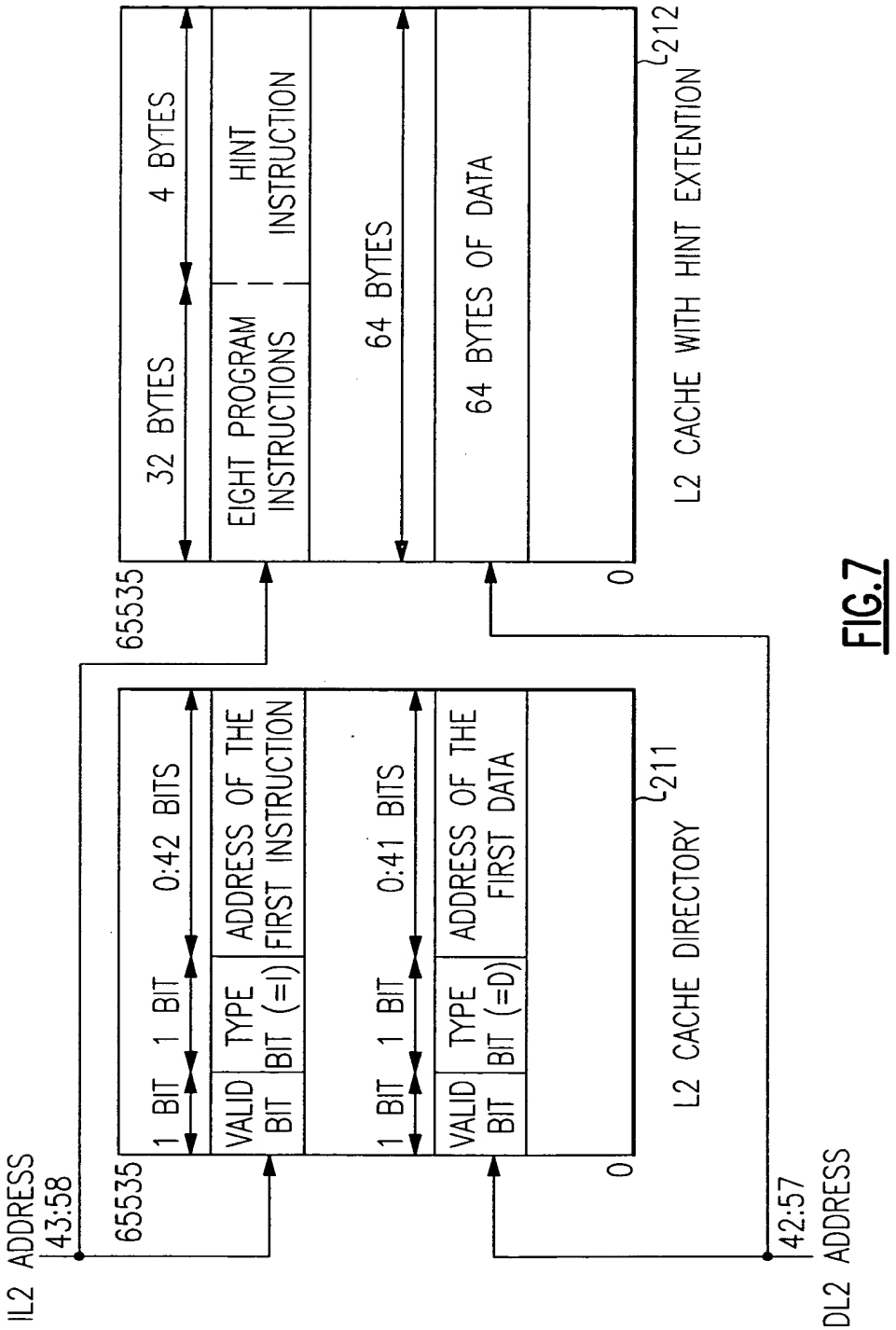

IL2 ADDRESS
43:58
65535
1 BIT
1 BIT
0:42 BITS
VALID BIT
TYPE BIT (=I)
ADDRESS OF THE FIRST INSTRUCTION
0
1 BIT
1 BIT
0:41 BITS
VALID BIT
TYPE BIT (=D)
ADDRESS OF THE FIRST DATA
0
L2 CACHE DIRECTORY
211
42:57
DL2 ADDRESS
65535
32 BYTES
4 BYTES
EIGHT PROGRAM INSTRUCTIONS
HINT INSTRUCTION
64 BYTES
64 BYTES OF DATA
0
L2 CACHE WITH HINT EXTENTION
212

FIG.7

FIG. 8A
FIG. 8B

FIG.8

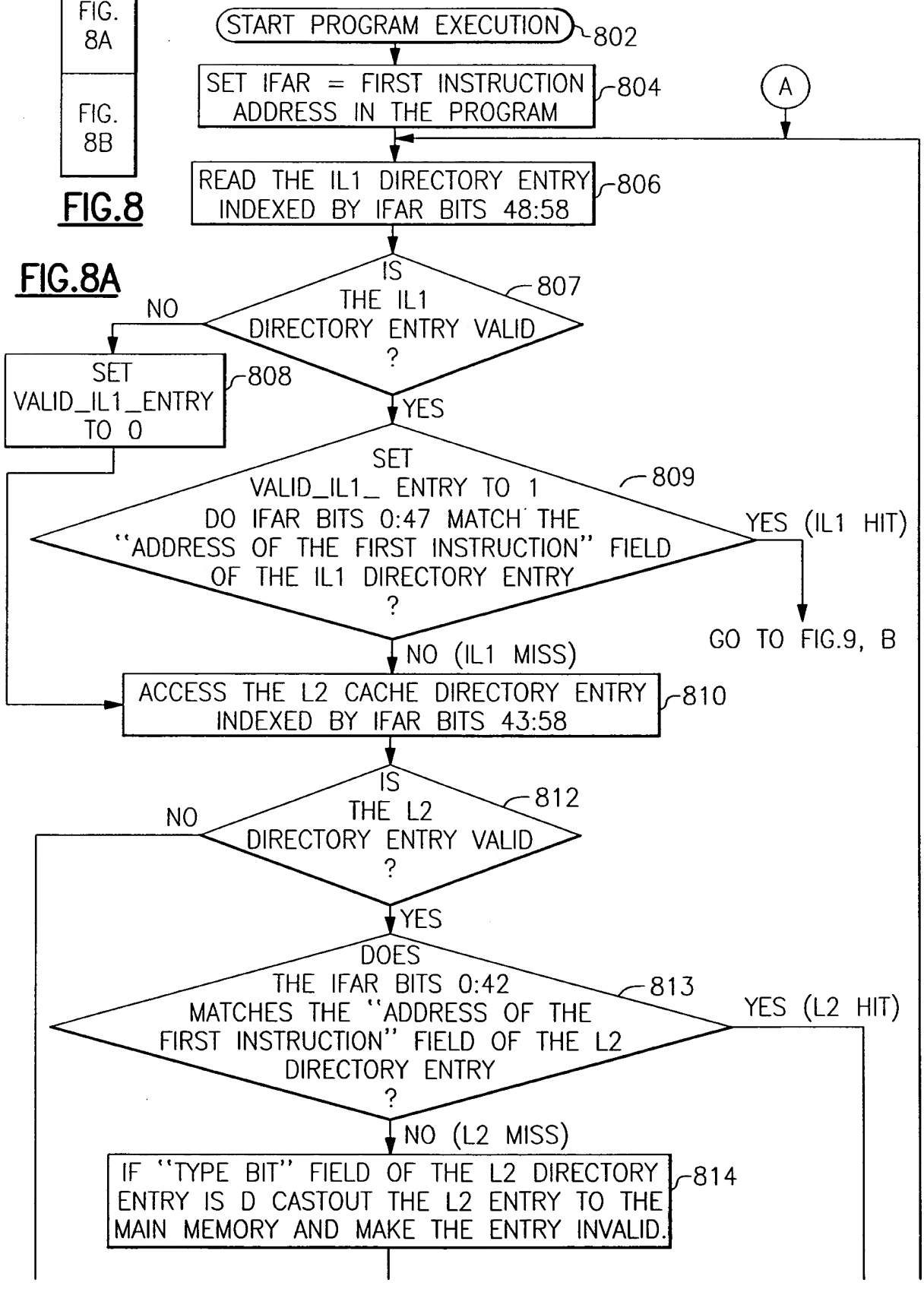


FIG.8A

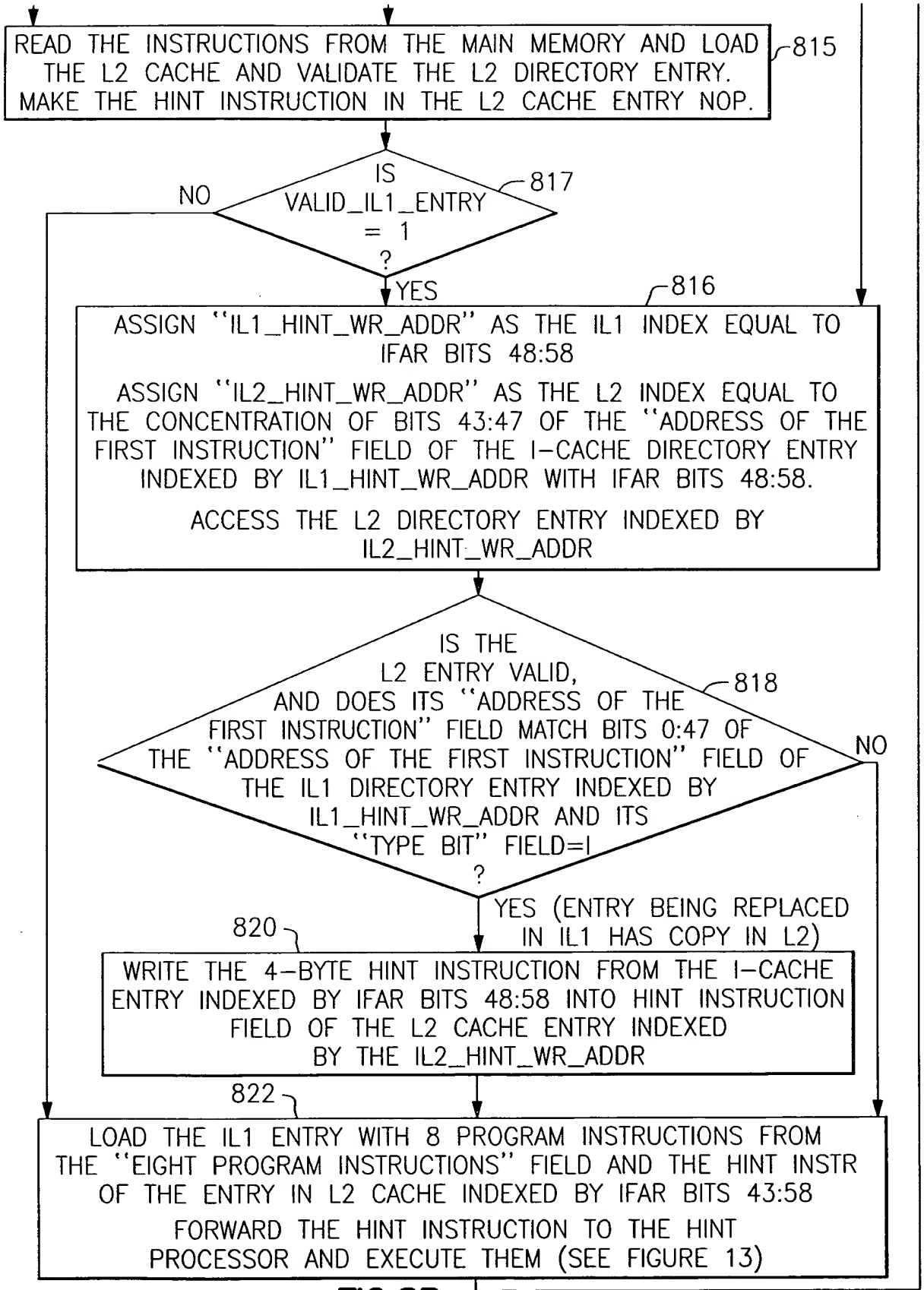

READ THE INSTRUCTIONS FROM THE MAIN MEMORY AND LOAD THE L2 CACHE AND VALIDATE THE L2 DIRECTORY ENTRY. MAKE THE HINT INSTRUCTION IN THE L2 CACHE ENTRY NOP.
815
IS VALID_IL1_ENTRY = 1 ?
817
NO
YES
816
ASSIGN "IL1_HINT_WR_ADDR" AS THE IL1 INDEX EQUAL TO IFAR BITS 48:58
ASSIGN "IL2_HINT_WR_ADDR" AS THE L2 INDEX EQUAL TO THE CONCENTRATION OF BITS 43:47 OF THE "ADDRESS OF THE FIRST INSTRUCTION" FIELD OF THE I-CACHE DIRECTORY ENTRY INDEXED BY IL1_HINT_WR_ADDR WITH IFAR BITS 48:58.
ACCESS THE L2 DIRECTORY ENTRY INDEXED BY IL2_HINT_WR_ADDR
IS THE L2 ENTRY VALID, AND DOES ITS "ADDRESS OF THE FIRST INSTRUCTION" FIELD MATCH BITS 0:47 OF THE "ADDRESS OF THE FIRST INSTRUCTION" FIELD OF THE IL1 DIRECTORY ENTRY INDEXED BY IL1_HINT_WR_ADDR AND ITS "TYPE BIT" FIELD=1 ?
818
NO
YES (ENTRY BEING REPLACED IN IL1 HAS COPY IN L2)
820
WRITE THE 4-BYTE HINT INSTRUCTION FROM THE I-CACHE ENTRY INDEXED BY IFAR BITS 48:58 INTO HINT INSTRUCTION FIELD OF THE L2 CACHE ENTRY INDEXED BY THE IL2_HINT_WR_ADDR
822
LOAD THE IL1 ENTRY WITH 8 PROGRAM INSTRUCTIONS FROM THE "EIGHT PROGRAM INSTRUCTIONS" FIELD AND THE HINT INSTR OF THE ENTRY IN L2 CACHE INDEXED BY IFAR BITS 43:58
FORWARD THE HINT INSTRUCTION TO THE HINT PROCESSOR AND EXECUTE THEM (SEE FIGURE 13)

FIG.8B

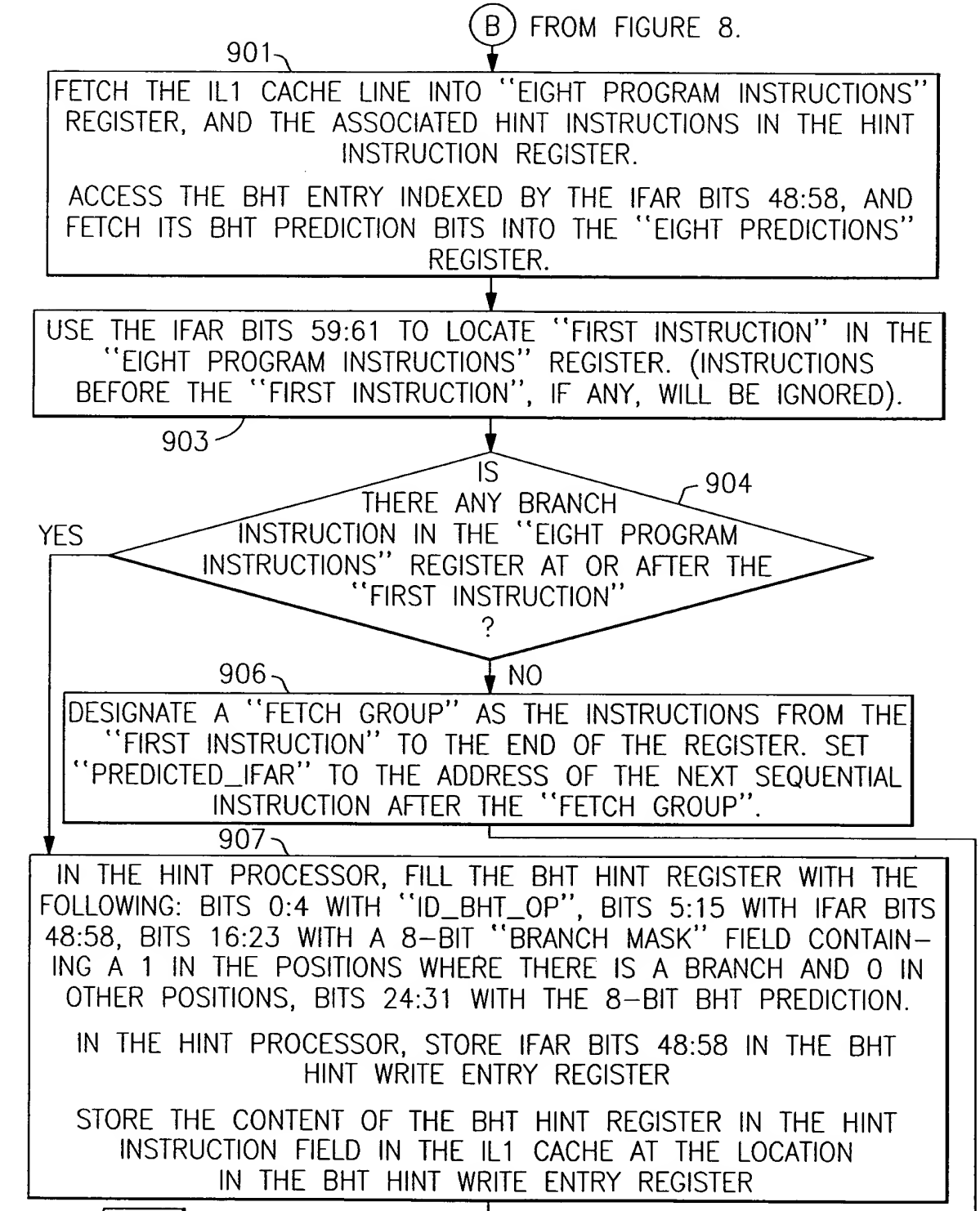


FIG.9

FIG. 9A

FIG. 9B

FIG.9A

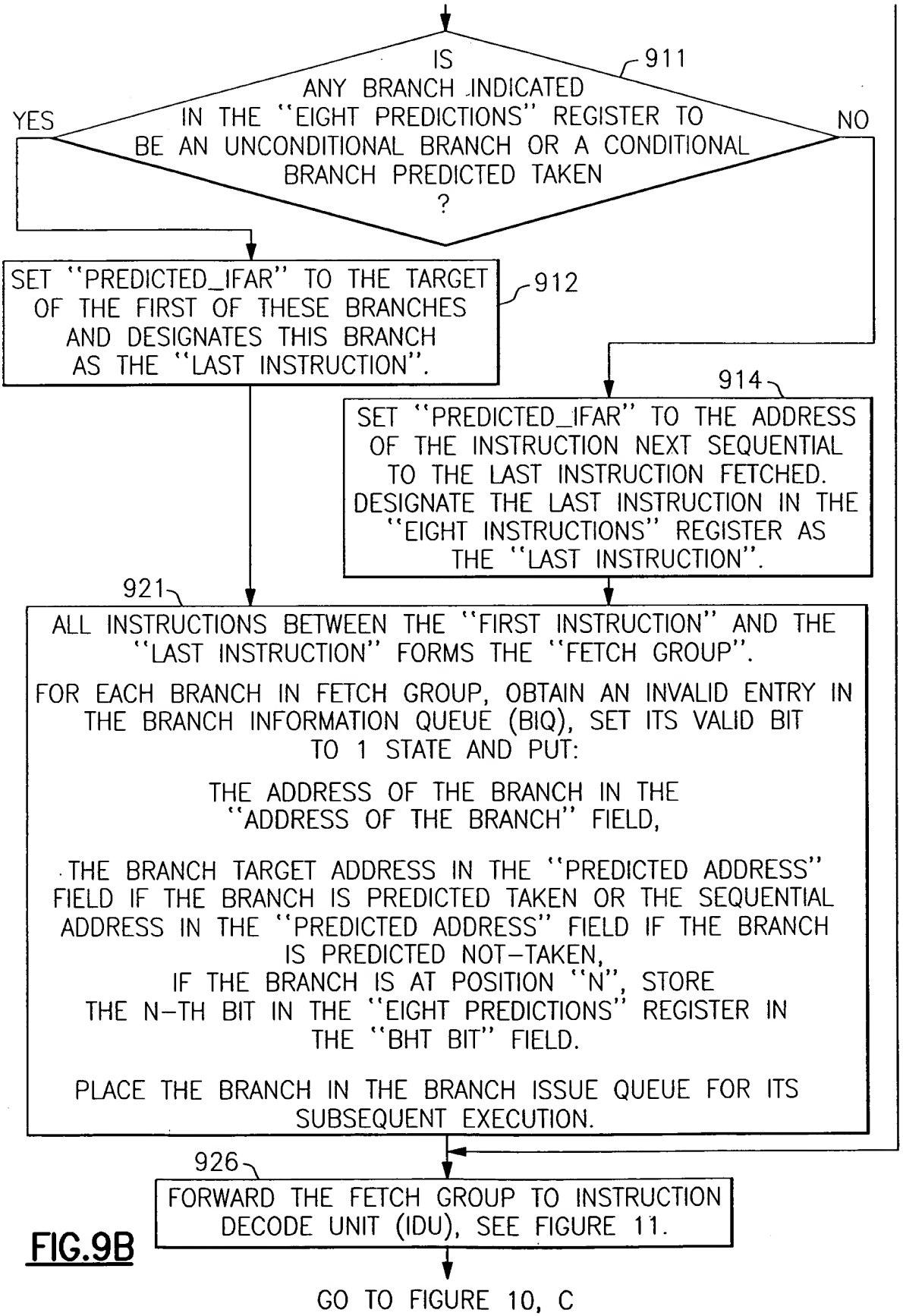

IS
ANY BRANCH INDICATED
IN THE "EIGHT PREDICTIONS" REGISTER TO
BE AN UNCONDITIONAL BRANCH OR A CONDITIONAL
BRANCH PREDICTED TAKEN
?
911
YES
NO
SET "PREDICTED_IFAR" TO THE TARGET
OF THE FIRST OF THESE BRANCHES
AND DESIGNATES THIS BRANCH
AS THE "LAST INSTRUCTION".
912
914
SET "PREDICTED_IFAR" TO THE ADDRESS
OF THE INSTRUCTION NEXT SEQUENTIAL
TO THE LAST INSTRUCTION FETCHED.
DESIGNATE THE LAST INSTRUCTION IN THE
"EIGHT INSTRUCTIONS" REGISTER AS
THE "LAST INSTRUCTION".
921
ALL INSTRUCTIONS BETWEEN THE "FIRST INSTRUCTION" AND THE
"LAST INSTRUCTION" FORMS THE "FETCH GROUP".
FOR EACH BRANCH IN FETCH GROUP, OBTAIN AN INVALID ENTRY IN
THE BRANCH INFORMATION QUEUE (BIQ), SET ITS VALID BIT
TO 1 STATE AND PUT:
THE ADDRESS OF THE BRANCH IN THE
"ADDRESS OF THE BRANCH" FIELD,
THE BRANCH TARGET ADDRESS IN THE "PREDICTED ADDRESS"
FIELD IF THE BRANCH IS PREDICTED TAKEN OR THE SEQUENTIAL
ADDRESS IN THE "PREDICTED ADDRESS" FIELD IF THE BRANCH
IS PREDICTED NOT-TAKEN,
IF THE BRANCH IS AT POSITION "N", STORE
THE N-TH BIT IN THE "EIGHT PREDICTIONS" REGISTER IN
THE "BHT BIT" FIELD.
PLACE THE BRANCH IN THE BRANCH ISSUE QUEUE FOR ITS
SUBSEQUENT EXECUTION.
926
FORWARD THE FETCH GROUP TO INSTRUCTION
DECODE UNIT (IDU), SEE FIGURE 11.
GO TO FIGURE 10, C

FIG.9B

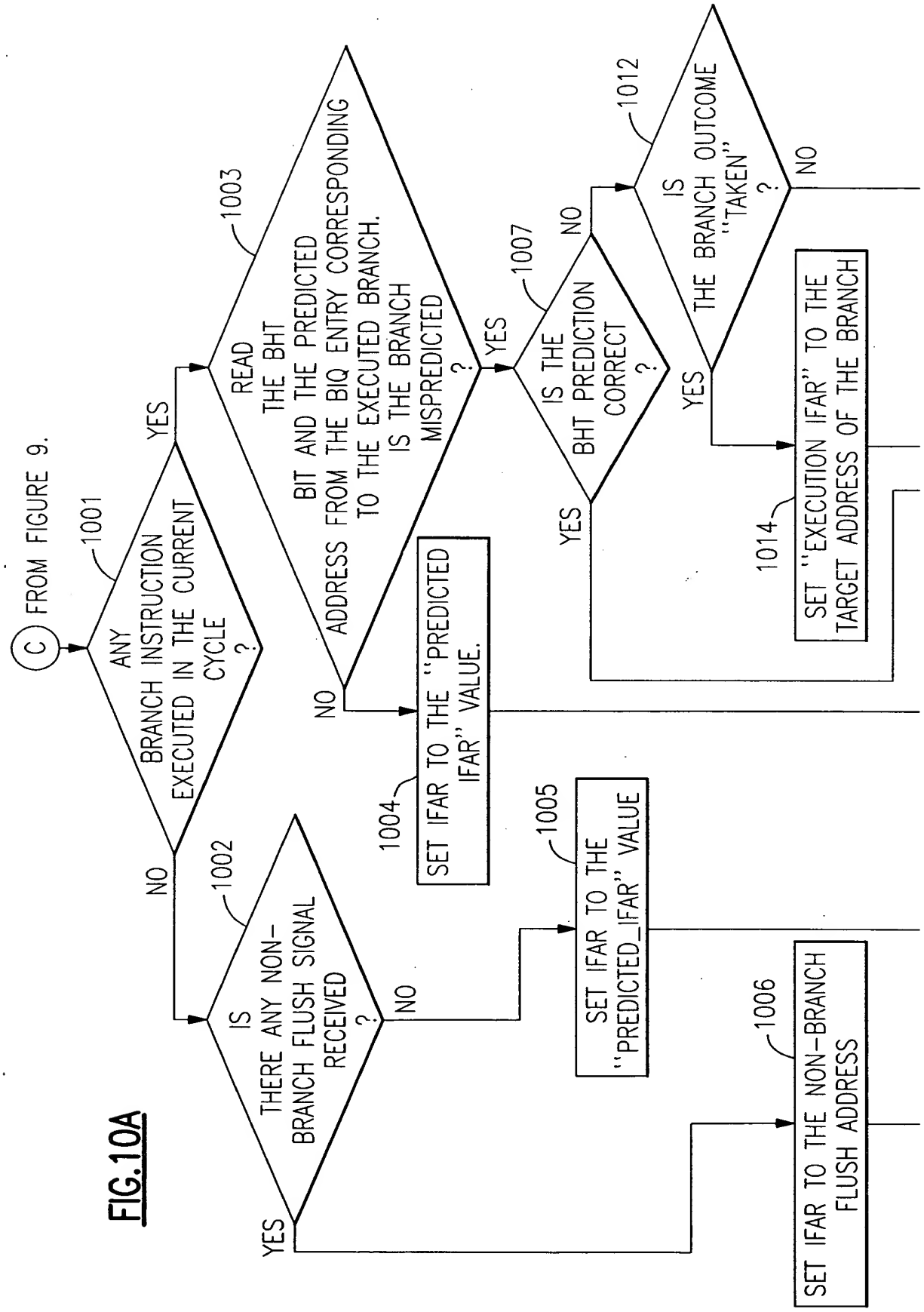

C FROM FIGURE 9.
1001
ANY BRANCH INSTRUCTION EXECUTED IN THE CURRENT CYCLE ?
YES
NO
1002
IS THERE ANY NON-BRANCH FLUSH SIGNAL RECEIVED ?
YES
NO
1003
READ THE BHT BIT AND THE PREDICTED ADDRESS FROM THE BIQ ENTRY CORRESPONDING TO THE EXECUTED BRANCH. IS THE BRANCH MISPREDICTED ?
YES
NO
1004
SET IFAR TO THE "PREDICTED IFAR" VALUE.
1005
SET IFAR TO THE "PREDICTED_IFAR" VALUE
1006
SET IFAR TO THE NON-BRANCH FLUSH ADDRESS
1007
IS THE BHT PREDICTION CORRECT ?
YES
NO
1012
IS THE BRANCH OUTCOME "TAKEN" ?
YES
NO
1014
SET "EXECUTION IFAR" TO THE TARGET ADDRESS OF THE BRANCH

FIG.10A

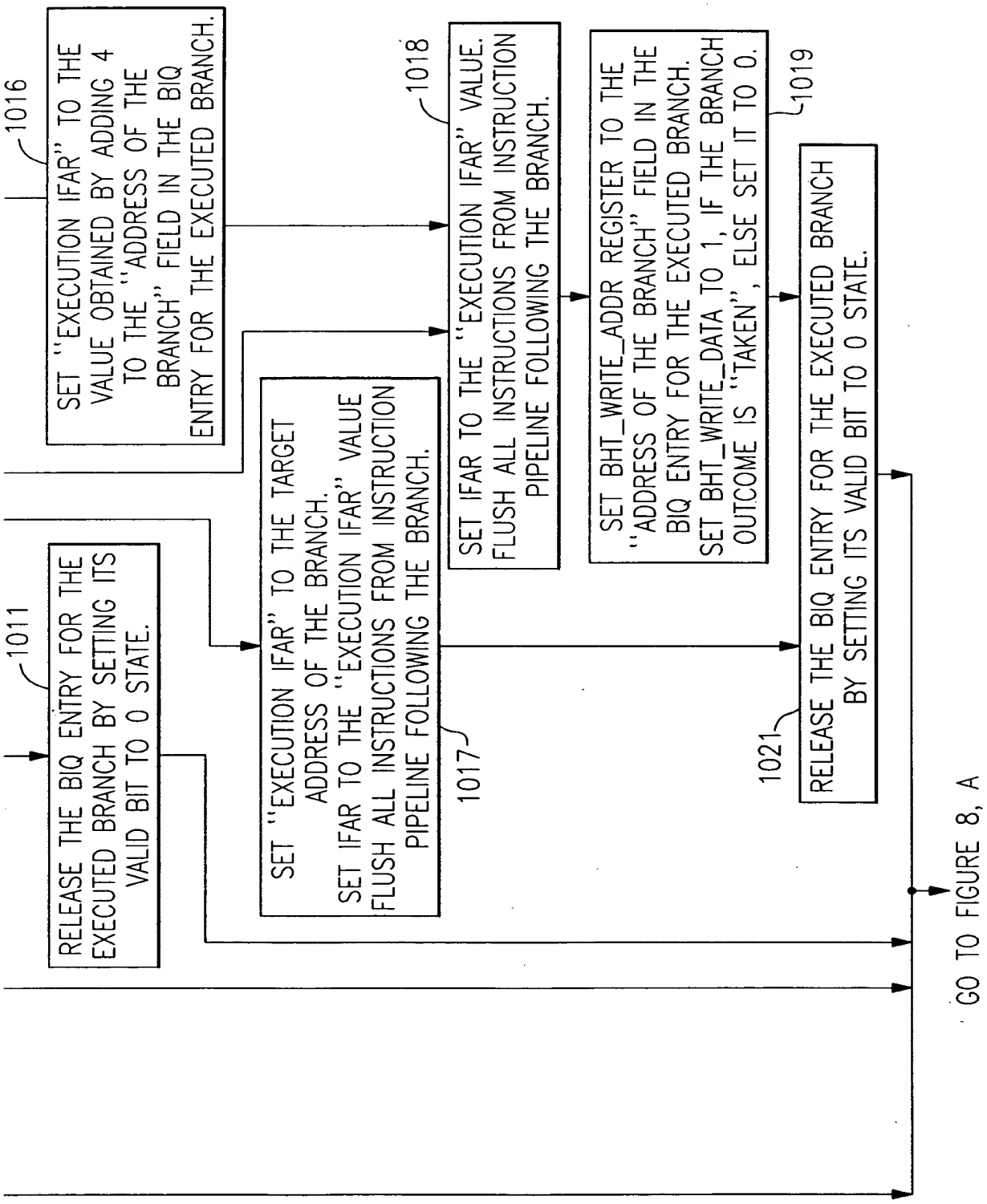


FIG. 10A | FIG. 10B

FIG.10

FIG.10B

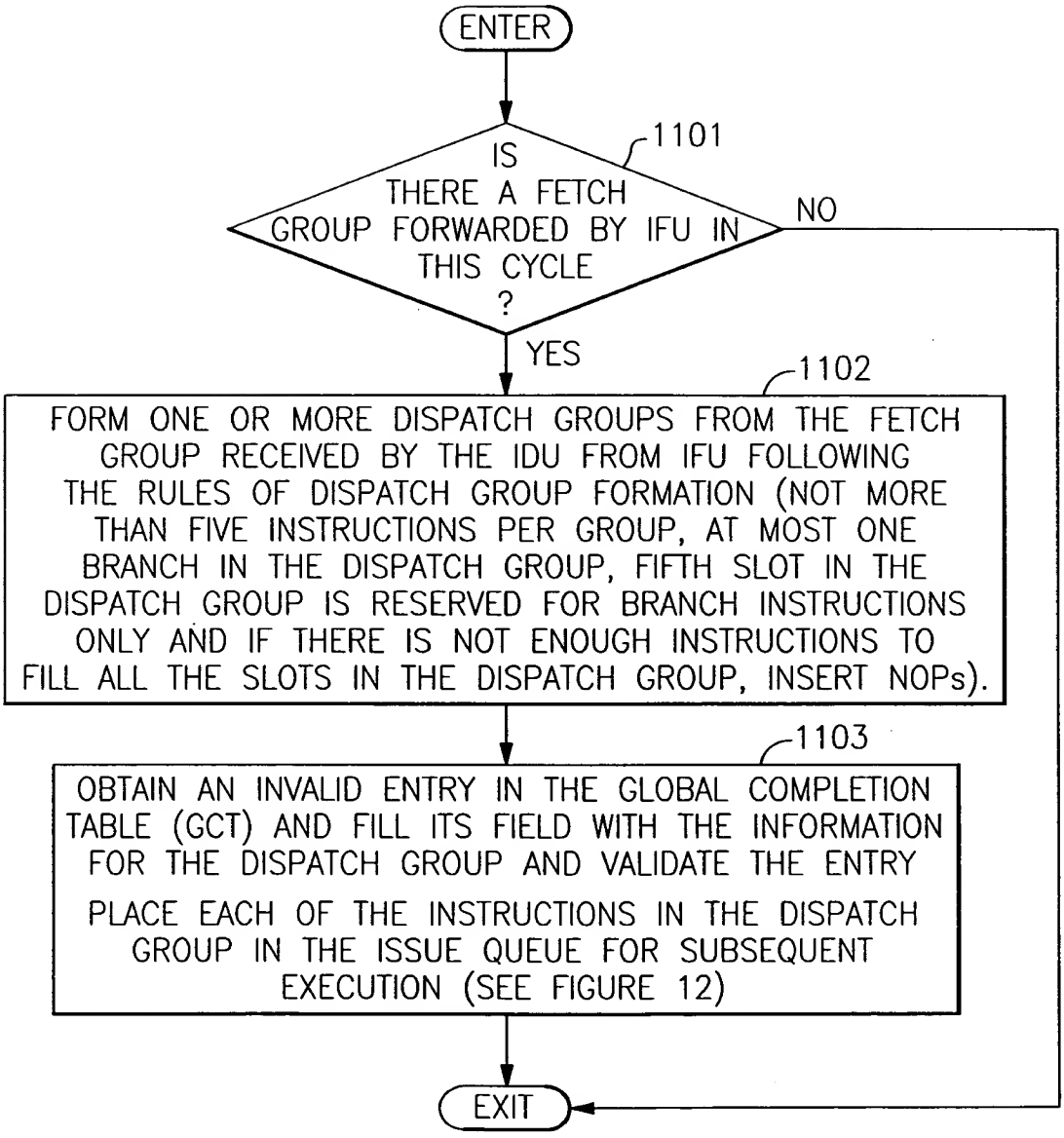

ENTER
1101
IS THERE A FETCH GROUP FORWARDED BY IFU IN THIS CYCLE ?
NO
YES
1102
FORM ONE OR MORE DISPATCH GROUPS FROM THE FETCH GROUP RECEIVED BY THE IDU FROM IFU FOLLOWING THE RULES OF DISPATCH GROUP FORMATION (NOT MORE THAN FIVE INSTRUCTIONS PER GROUP, AT MOST ONE BRANCH IN THE DISPATCH GROUP, FIFTH SLOT IN THE DISPATCH GROUP IS RESERVED FOR BRANCH INSTRUCTIONS ONLY AND IF THERE IS NOT ENOUGH INSTRUCTIONS TO FILL ALL THE SLOTS IN THE DISPATCH GROUP, INSERT NOPs).
1103
OBTAIN AN INVALID ENTRY IN THE GLOBAL COMPLETION TABLE (GCT) AND FILL ITS FIELD WITH THE INFORMATION FOR THE DISPATCH GROUP AND VALIDATE THE ENTRY
PLACE EACH OF THE INSTRUCTIONS IN THE DISPATCH GROUP IN THE ISSUE QUEUE FOR SUBSEQUENT EXECUTION (SEE FIGURE 12)
EXIT

FIG.11

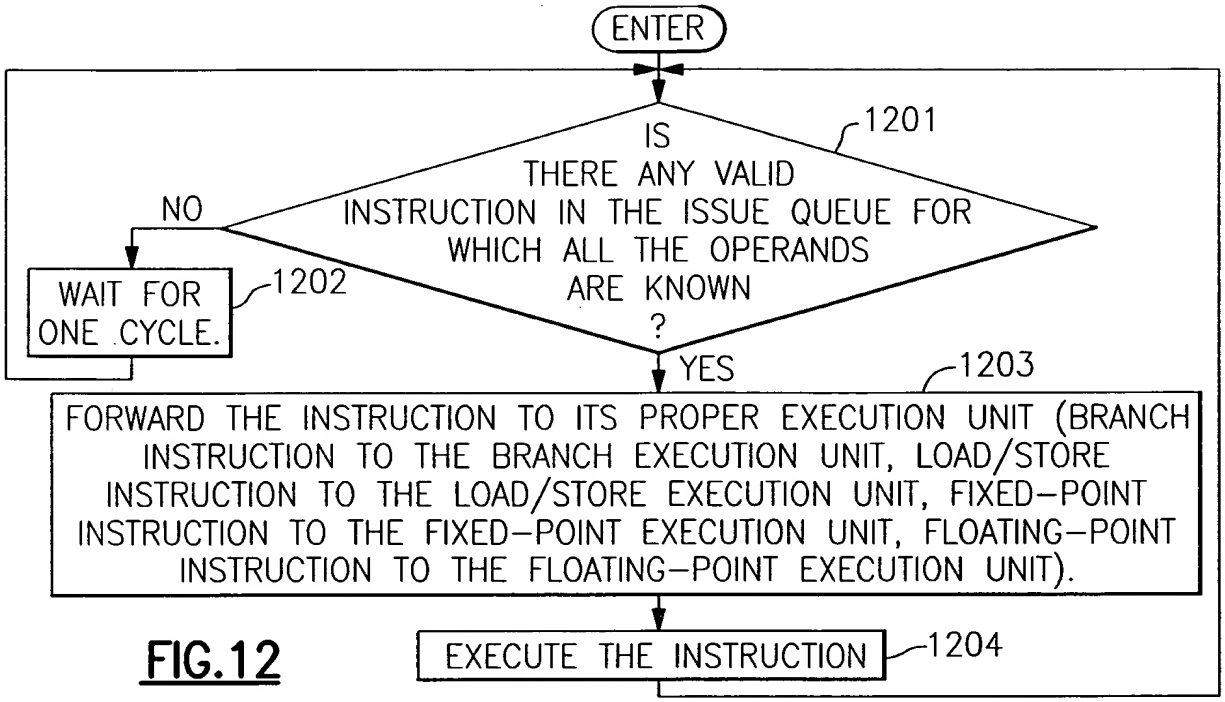

ENTER
IS THERE ANY VALID INSTRUCTION IN THE ISSUE QUEUE FOR WHICH ALL THE OPERANDS ARE KNOWN ?
1201
NO
WAIT FOR ONE CYCLE.
1202
YES
1203
FORWARD THE INSTRUCTION TO ITS PROPER EXECUTION UNIT (BRANCH INSTRUCTION TO THE BRANCH EXECUTION UNIT, LOAD/STORE INSTRUCTION TO THE LOAD/STORE EXECUTION UNIT, FIXED-POINT INSTRUCTION TO THE FIXED-POINT EXECUTION UNIT, FLOATING-POINT INSTRUCTION TO THE FLOATING-POINT EXECUTION UNIT).
EXECUTE THE INSTRUCTION
1204

FIG.12

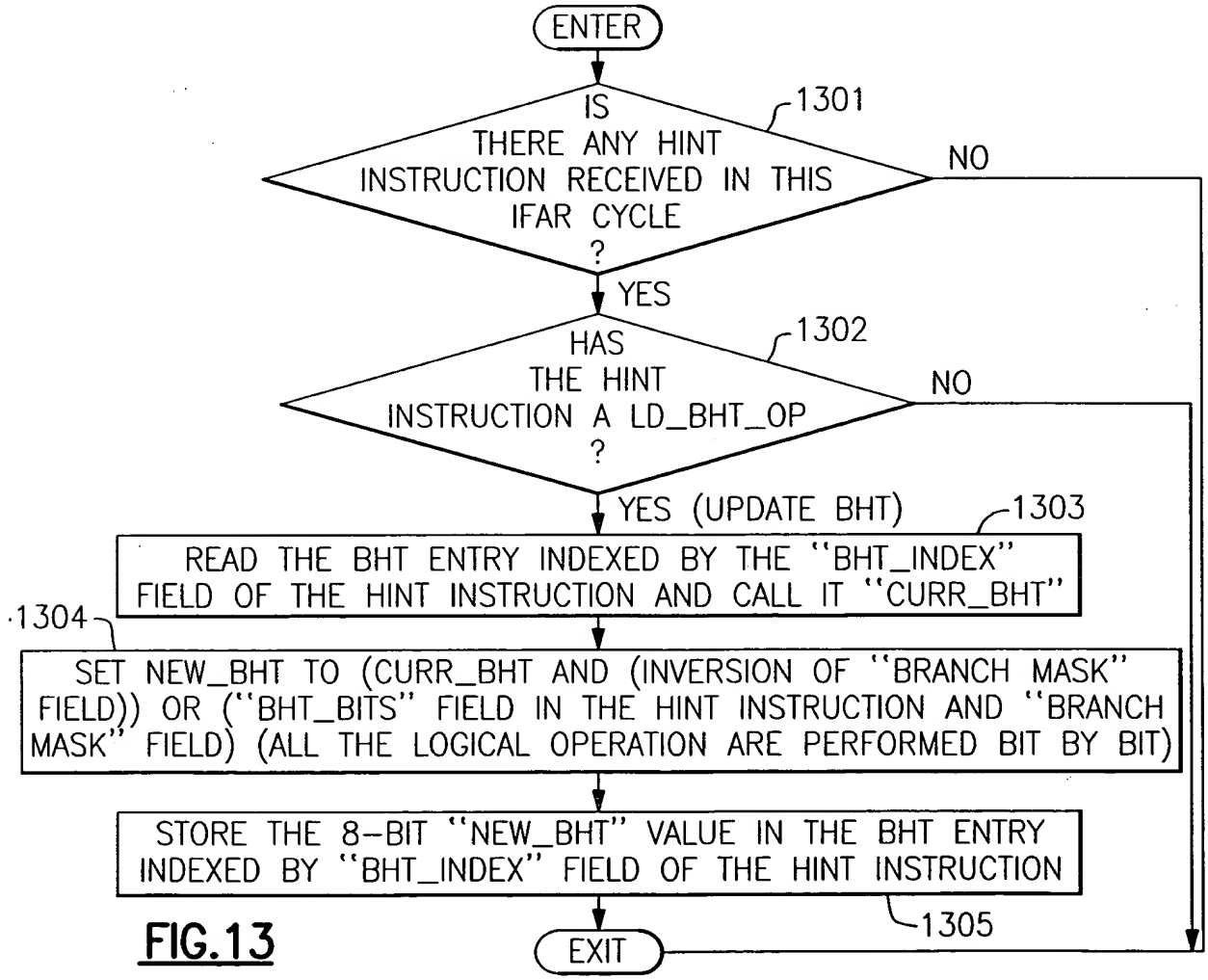

ENTER
IS THERE ANY HINT INSTRUCTION RECEIVED IN THIS IFAR CYCLE ?
1301
NO
YES
HAS THE HINT INSTRUCTION A LD_BHT_OP ?
1302
NO
YES (UPDATE BHT)
1303
READ THE BHT ENTRY INDEXED BY THE "BHT_INDEX" FIELD OF THE HINT INSTRUCTION AND CALL IT "CURR_BHT"
1304
SET NEW_BHT TO (CURR_BHT AND (INVERSION OF "BRANCH MASK" FIELD)) OR ("BHT_BITS" FIELD IN THE HINT INSTRUCTION AND "BRANCH MASK" FIELD) (ALL THE LOGICAL OPERATION ARE PERFORMED BIT BY BIT)
STORE THE 8-BIT "NEW_BHT" VALUE IN THE BHT ENTRY INDEXED BY "BHT_INDEX" FIELD OF THE HINT INSTRUCTION
1305
EXIT

FIG.13